United States Patent Application for:

METHOD OF IMPROVING THE UNIFORMITY OF A PATTERNED RESIST ON A PHOTOMASK

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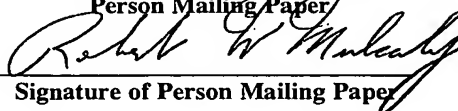
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[0001]   **METHOD OF IMPROVING THE UNIFORMITY OF A PATTERNED RESIST ON A PHOTOMASK**

3   [0002]   1.   Field of the Invention

4   [0003]   In general, the present invention relates to a method of producing a photomask

5   (reticle) for use in the semiconductor industry. In particular, the invention pertains to a

6   method for improving the critical dimension (CD) uniformity of a pattern in a photoresist

7   which is used to transfer the pattern to a reticle.

8   [0004]   2.   Brief Description of the Background Art

9   [0005]   Photoresists are used in microlithographic processes to produce patterned features

10   required for device functioning in miniaturized electronic components, such as in the

11   fabrication of semiconductor device structures. The miniaturized electronic device structure

12   patterns are typically created using blanket radiation through a photomask to produce a

13   pattern in a layer of photoresist material present on a semiconductor structure. There are

14   instances, for specialized devices, where a pattern is directly written into a photoresist

15   present on the semiconductor structure; however, due to the slow production speed of the

16   direct write process, this is not commonly done.

17   [0006]   A photomask or reticle which is used to enable rapid semiconductor device

18   processing typically includes a thin layer of a radiation-blocking material (which is often a

19   metal-containing material, such as a chrome-containing, molybdenum-containing, or

20   tungsten-containing layer, for example) deposited on a glass or quartz plate. The thin layer

21   of radiation-blocking material is patterned to contain a "hard copy" of the pattern to be

22   recreated on the photoresist or photoresist / hard mask layer overlying a semiconductor

23   structure. The patterning of the radiation-blocking layer of a reticle may be carried out using

24   a number of different techniques. Due to the dimensional requirements of today's

25   semiconductor structures, the pattern is typically generated using a direct write laser or

26   e-beam to create a latent image in a photoresist for subsequent transfer to the radiation-

1   blocking layer.

2   [0007]   The reticle manufacturing process generally includes the following steps, when

3   the initial substrate used to form the reticle is a silicon oxide-containing base layer having

4   a layer of a metal-containing (typically chrome) mask material applied thereover: An

5   inorganic antireflective coating (ARC) or an organic ARC, or a combination of inorganic

6   and organic ARC layers, may be applied over the surface of the chrome mask material. A

7   photoresist layer is then applied over the antireflective coating. The photoresist is typically

8   an organic material which is dissolved in a solvent.   The solution of photoresist is typically

9   spin coated onto the surface of the photomask fabrication structure. Some of the solvent is

10   removed during the spin coating operation. Residual solvent is subsequently removed by

11   another means, typically by baking the fabrication structure, including the photoresist layer.

12   This step is commonly referred to as a "post-apply bake" or PAB.   The photoresist is then

13   exposed to radiation (imaged), to produce a pattern in the photoresist layer, typically by a

14   direct write process when the pattern includes dimensions which are less than about 0.4 μm

15   or less. After exposure, the substrate including the photoresist layer is baked again. The

16   second baking is typically referred to as a "post-exposure bake" or PEB. The photoresist

17   is then developed, either using a dry process or a wet process, to create the pattern having

18   openings through the photoresist layer thickness. Once the photoresist is "patterned" so that

19   the pattern openings extend through the photoresist layer to the upper surface of an ARC

20   layer, or to a surface beneath an ARC layer, the pattern in the patterned photoresist is

21   transferred through the chrome-based mask layer and any remaining layers overlying the

22   chrome layer, for example, typically by dry etching.

23   [0008]   As described above, preparation of a photomask / reticle is a complicated process

24   involving a number of interrelated steps which affect the critical dimensions of a pattern

25   produced in the reticle and the uniformity of the pattern critical dimensions across the

26   surface area of the reticle. Various efforts have been made within the industry to improve

27   the reliability of manufacturing processes by improving individual process steps; however,

28   when a production process involves a number of interrelated process steps, alteration of an

1   individual process step may have an unexpected result on other interrelated process steps.

2   [0009]   Commonly owned U.S. Patent No. 6,703,169, to Scott Fuller et al., issued March

3   9, 2004, and entitled "Method of Preparing Optically Imaged High Performance

4   Photomasks", discloses a state-of-the-art method of fabricating a photomask using optical

5   radiation in the form of a direct write continuous wave laser. The claimed method

6   comprises a series of steps including: applying an organic antireflection coating over a

7   metal-containing layer; applying a chemically-amplified positive tone or negative tone DUV

8   photoresist over the organic antireflection coating, to provide a photoresist-coated

9   photomask substrate; post-apply baking the DUV photoresist over a temperature ranging

10   from about 105°C to about 115°C; exposing a surface of the DUV photoresist to radiation

11   from the direct write continuous wave laser, to provide a patterned photoresist across the

12   photomask substrate; and post-exposure baking the DUV photoresist over a temperature

13   ranging from about 70°C to about 90°C. The post-apply bake process provides increased

14   stability period for the photoresist-coated photomask substrate, where there is less than a

15   5 nm change in a 400 nm latent image critical dimension after a 6-hour time period. A

16   combination of the post-apply bake process and the post-exposure bake process results in

17   a uniform critical dimension of the patterned photoresist across the photomask substrate,

18   where, for a 132-mm x 132-mm active area, a critical dimension uniformity is $\leq$ 10 nm at

19   400 nm. The disclosure of U.S. Patent No. 6,703,169 is hereby incorporated by reference

20   in its entirety.

21   [0010]   Commonly owned, co-pending U.S. Application Serial No. 10/768,919, of

22   Christopher Dennis Bencher et al., filed January 30, 2004, and entitled "Reticle Fabrication

23   Using a Removable Hard Mask", discloses a method of fabricating a reticle which provides

24   improved critical dimension uniformity during fabrication of a reticle by minimizing the

25   problem known as "photoresist pull-back", which commonly occurs during etching of a

26   chrome (or other radiation-blocking layer) on a reticle substrate. According to the method

27   disclosed by Bencher et al., pattern transfer to the radiation-blocking layer of the reticle

28   substrate essentially depends upon transfer from a hard mask rather than from a photoresist.

1   In one embodiment, a hard mask material having anti-reflective properties is left on the

2   surface of the chrome after etching of the chrome. Since the hard mask surface faces the

3   surface of a photoresist on the semiconductor substrate which is patterned using the reticle,

4   the presence of the proper anti-reflective properties in the hard mask can be used to reduce

5   the amount of bounce-back of reflected radiation which occurs during blanket radiation

6   imaging of the semiconductor photoresist through the reticle. In another embodiment, where

7   a wet etch is used during fabrication of the reticle, the hard mask material (whether having

8   anti-reflective properties or not) is removed to prevent contamination during the wet etch

9   process. In this embodiment, when a plasma etchant used to remove the hard mask would

10   also etch the reticle base substrate (which is typically quartz), a protective layer is applied

11   to fill at least a portion of patterned openings through the chrome during removal of the hard

12   mask. This prevents etching of the quartz at the bottom of the pattern openings during

13   removal of the hard mask. The disclosure of U.S. Application Serial No. 10/768,919 is

14   hereby incorporated by reference in its entirety.

15   [0011]   As device dimensions become even smaller, further improvements in critical

16   dimension uniformity of photomasks are needed. One commonly used means of improving

17   photomask dimensional uniformity is by improving the dimensions of the patterned

18   photoresist used to transfer the pattern to the photomask. The patterned photomask may be

19   "descummed" using an oxygen plasma step, in which surface defects are removed from the

20   photoresist pattern. Exposure to the oxygen plasma basically burns away a fixed amount

21   of resist, which may help to smooth pattern line edges. Unfortunately, however, the descum

22   oxygen plasma step typically reduces the resist dimensions by about 20 - 30 nm, making the

23   descum process inapplicable to very small feature lithography.

24   [0012]   It is readily apparent that it would be highly desirable to have a method of making

25   a photomask where the uniformity of pattern critical dimensions is maintained across the

26   entire surface of the photomask, even for features smaller than about 100 nm. To provide

27   an improved photomask, it would be very advantageous to provide an improved patterned

28   photoresist which can be used to transfer the pattern directly to the photomask, or to transfer

1   the pattern to a hard mask which is subsequently used to pattern the photomask.

2   [0013]   **SUMMARY OF THE INVENTION**

3   [0014]   We have discovered that application of a vacuum to a pattern irradiated (imaged)

4   photoresist prior to development of the photoresist provides an improvement in critical

5   dimension and uniformity in the developed photoresist. This improvement is translated into

6   an improvement in the patterned photomask produced using the photoresist.

7   [0015]   Typically, the application of vacuum is carried out prior to a post-exposure bake

8   of the kind which is commonly performed on an imaged photoresist prior to development.

9   Exposure of the photoresist on the photomask substrate to vacuum is performed for a period

10   of time sufficient to allow the imaged pattern critical dimensions to reach equilibrium across

11   the photoresist. The vacuum treatment process allows reaction by-product, water vapor, and

12   solvents, for example, to desorb from the surface of the resist, improving critical dimension

13   uniformity across the surface of the photoresist on the photomask substrate.

14   [0016]   Typically, exposure of the pattern-imaged photoresist to vacuum is performed at

15   a substrate temperature within the range of about 18°C to about 60°C (more typically,

16   within the range of about 18°C to about 40°C), for a period of time within the range of

17   about 10 minutes to about 70 hours (more typically, within the range of about 20 minutes

18   to about 12 hours), at a process chamber pressure ranging from about 5 x 10^{-6} mTorr to

19   about 5 mTorr. The pressure within the processing chamber during the vacuum treatment

20   process may be limited by the capability of the particular apparatus in which the vacuum

21   treatment process is performed. For example, when the vacuum treatment process is

22   performed in an Applied Materials' MEBES™ QUADRA™ or MEBES™ eXara™ e-beam

23   direct-write apparatus following the pattern writing process, the process chamber pressure

24   during the vacuum treatment process is typically about 1 x 10^{-5} mTorr. When the vacuum

25   treatment process is performed in an Applied Materials' TETRA™ etch system, the process

26   chamber pressure during the vacuum treatment process may vary between about 10^{-7} Torr

27   to about 10 mTorr, and was typically in the range of about 0.5 mTorr to about 1 mTorr

1   during the experimentation described herein.

2   [0017]   The time period required for pattern critical dimensions to reach equilibrium

3   across the photoresist will depend upon the photoresist layer composition, and a

4   combination of the temperature of the substrate / photoresist during the vacuum treatment

5   process and the pressure (vacuum) applied. The minimal time period required for vacuum

6   treatment of the photoresist on the photomask substrate will be the time period which

7   provides no substantial change in pattern critical dimensions upon continued exposure of the

8   irradiated photoresist to the vacuum.

9   [0018]   Typically, the higher the temperature, the less time is required for pattern critical

10   dimensions to reach equilibrium. However, the temperature is limited by the general

11   stability of the photoresist material, which will depend on the particular photoresist material

12   used. Also, typically the lower the pressure in the process chamber, the less time is required

13   for vacuum treatment at a given temperature; however, the pressure used must ensure that

14   deformation of the pattern does not occur and that the integrity of the photoresist is

15   preserved. The amount of time required will also depend upon the condition of the

16   photoresist prior to the vacuum treatment process, which will depend upon the type of

17   photoresist used, the solvents in the photoresist, and the length of time of the post-apply

18   bake (PAB) process. With minimal experimentation, one skilled in the art will be able to

19   integrate the vacuum treatment step into an existing process for photomask production.

20   [0019]   We have also discovered that exposure of the patterned (developed) photoresist

21   to vacuum after development results in an improvement in the line edge roughness of pattern

22   openings that have been formed through the photoresist layer thickness. This second

23   vacuum treatment process is typically performed at a substrate temperature within the range

24   of about 20°C to about 60°C for a period of time within the range of about 10 minutes to

25   about 60 minutes, at a process chamber pressure ranging from about 5×10^{-6} mTorr to about

26   5 mTorr, where the time period is a function of the combination of temperature and pressure.

27   In this second vacuum treatment, water vapor and solvents absorbed during the development

28   process are desorbed from surfaces of the patterned resist, including the sidewalls and top

1   resist surface. During desorption of the volatile components, the portion of the resist which

2   is close to the surface is placed in tension. It is theorized, but not intended as a limitation,

3   that this surface tension may allow for the "pulling together" of the surface, which may

4   smooth out sidewall roughness. Since the bulk of the resist (deeper than within a few

5   nanometers of the surface) is not in tension, lines and other features are not distorted.

6   [0020]   The vacuum treatment processes of the invention work well whether the

7   photoresist on the photomask substrate has been exposed to electron beam (e-beam) or

8   optical radiation. Vacuum processing of photomask substrates according to the method of

9   the invention typically improves the mean CD of the patterned photoresist by reducing the

10   variation from the intended CD by about 3 nm or more, and by improving the uniformity

11   (3-sigma) across a substrate surface by about 3 - 5 nm.

12   [0021]   **BRIEF DESCRIPTION OF THE DRAWINGS**

13   [0022]   Figure 1A shows a schematic cross-sectional view of a typical embodiment of a

14   beginning structure 100 of a stack of materials used in the production of a photomask or

15   reticle, when the pattern is transferred from the photoresist to the radiation-blocking layer

16   of the mask without the use of a hard mask. The stack from bottom to top includes a

17   substrate 102, which is typically selected from quartz, fluorinated quartz, borosilicate glass,

18   or soda lime glass; a radiation-blocking layer 104, which is typically a metal-containing

19   layer selected from a chromium, molybdenum silicide, or tungsten-containing layer, or

20   combinations thereof (in the examples described herein, the radiation-blocking layer is

21   essentially chrome); an inorganic ARC layer 105; an organic ARC layer 106; and a

22   photoresist layer 108.

23   [0023]   Figure 1B shows the Figure 1A structure 100 after development of the photoresist

24   layer 108 to create a pattern of lines and spaces in the photoresist layer 108.

1   [0024]   Figure 2 is a graph 200 showing a global cross·1 x CD uniformity (in nm)

2   following vacuum treatment of the imaged photoresist prior to development, when the

3   substrates were vacuum treated in a MEBES™ QUADRA™ imaging system ("RSB

4   Vacuum Treated") or were vacuum treated in an Applied Materials' TETRA™ etch chamber

5   ("Tetra Vacuum Treated"), compared with the global CD uniformity for substrates which

6   received no vacuum treatment following exposure of the photoresist to radiation ("No

7   Vacuum").

8   [0025]   Figure 3 is a graph 300 showing the decrease in developed photoresist thickness

9   302 as a function of time under vacuum 304, for photomask substrates which were vacuum

10   treated in accordance with the present invention. The substrates were vacuum treated in an

11   Applied Materials' TETRA™ etch chamber, at a temperature of approximately 45°C and

12   a process chamber pressure of approximately 0.5 mTorr.

13   [0026]   Figure 4 is a graph 400 showing local CD uniformity (in nm) before and after

14   vacuum treatment of the developed photoresist. The substrates were vacuum treated in an

15   Applied Materials' TETRA™ etch chamber for a period of 20 minutes, at a temperature of

16   approximately 45°C and a process chamber pressure of approximately 1 mTorr.

17   [0027]   **DETAILED DESCRIPTION OF THE INVENTION**

18   [0028]   We have discovered a method of improving the patterning of a layer of

19   photoresist which has been applied over a photomask substrate, The present method results

20   in improved critical dimension uniformity of the developed photoresist. In general, the

21   method comprises the steps of: a) post-apply baking the photoresist; b) exposing the

22   photoresist to imaging radiation (typically direct-write radiation); c) exposing the imaged

23   photoresist to a vacuum for a period of time sufficient to allow pattern critical dimensions

24   to equilibrate across the photoresist, at a process chamber pressure ranging from about

25   5×10^{-6} mTorr to about 5 mTorr (typically, at a temperature ranging from about 20°C to

1   about 60°C, and for a time period ranging from about 10 minutes to about 70 hours);

2   d) post-exposure baking the imaged photoresist; and e) developing the imaged photoresist

3   to create a pattern having openings through the photoresist layer thickness.

4   [0029]   The method may further comprise the additional step f) of exposing the developed

5   photoresist to a vacuum subsequent to step e), at a substrate temperature within the range

6   of about 20°C to about 60°C for a period of time within the range of about 10 minutes to

7   about 60 minutes, at a process chamber pressure ranging from about 5×10^{-6} mTorr to about

8   5 mTorr. This second vacuum exposure step has been shown to improve the line edge

9   roughness of pattern openings that have been formed through the photoresist layer thickness.

10   [0030]   As a preface to the detailed description presented below, it should be noted that,

11   as used in this specification and the appended claims, the singular forms "a", "an", and "the"

12   include plural referents, unless the context clearly dictates otherwise.

13   [0031]   I.   <u>METHOD OF PATTERNING A PHOTORESIST ON A PHOTOMASK</u>
14   <u>SUBSTRATE</u>

15   [0032]   All methods of patterning a photomask substrate may benefit from application of

16   the present method. The method is particularly useful for DUV optical or e-beam patterning

17   of a photomask when a chemically amplified photoresist is used to transfer the pattern to the

18   photomask. The present Examples are for a REAP™ 200 chemically amplified photoresist

19   (available from Tokyo Ohka Kogyo Co., Ltd. (TOK), Kawasaki, Japan), which is useful

20   with both e-beam radiation and 248 nm optical radiation. However, the scope of the

21   invention is not intended to be limited to this family of chemically amplified photoresists.

22   [0033]   Figure 1A shows one embodiment of a starting structure 100 used in the

23   fabrication of example photomasks for experimental purposes herein. In this Example,

24   starting structure 100 was a stack of layers (not shown to scale) which included, from top

25   to bottom, a 3000 Å thick layer 108 of a chemically amplified photoresist, REAP™ 200

26   (available from TOK, Kawasaki, Japan); a 500 Å thick layer 106 of an organic ARC

27   identified as XLT-BARC (available from Brewer Science, Inc., Rolla, MO); a 300 Å thick

1   layer 105 of chromium oxynitride inorganic ARC; a 400 Å thick layer 104 of chrome mask

2   material; and a silicon oxide-containing substrate 102.

3   [0034]   The starting structure 100 shown in Figure 1A can be formed using conventional

4   deposition techniques known in the art of semiconductor manufacture. In particular, the

5   photoresist layer 108 is typically applied to the surface of the organic ARC layer 106 using

6   spin-on coating techniques. Some of the solvent or dispersion medium is removed during

7   the spin coating operation.

8   [0035]   Photoresist compositions of the kind suitable for use in the present method

9   include: REAP™ 200 and EN24 (both available from TOK, Kawasaki, Japan); NEB 22

10   (available from Sumitomo Chemical Co., Ltd., Tokyo, Japan); and FEP 171 and FEN 270

11   (both available from Fuji-Hunt Electronics Company, Tokyo, Japan), by way of example

12   and not by way of limitation.

13   [0036]   After application of the photoresist layer, applicants performed a post-apply bake

14   (PAB) process to remove residual solvent or dispersion medium. The post-apply bake

15   process is typically performed at a temperature within the range of about 70°C to about

16   150°C, for a time period of about 4 minutes to about 30 minutes. A particularly useful post-

17   apply bake process is described in detail in U.S. Patent No. 6,703,169, to Fuller et al., the

18   disclosure of which is incorporated by reference in its entirety.

19   [0037]   After post-apply bake, the photoresist was exposed to radiation (imaged), to

20   produce a latent pattern in the photoresist layer, typically by a direct write process when the

21   pattern includes dimensions which are less than about 0.4 μm. In the example embodiment,

22   the minimum pattern dimension was about 60 nm. In the exposure process, the integrated

23   circuit patterns were direct written onto the unpatterned photoresist 108 coated on a mask

24   blank which included organic ARC layer 106, inorganic ARC layer 105, chrome-containing

25   layer 104, and quartz layer 102 (described above). In a different embodiment, a hard mask

26   (not shown) may be present between the photoresist 108 and the radiation-blocking layer

27   104.

1 [0038]   The vacuum treatment process of the invention works well whether imaging of

2 the photoresist is by e-beam radiation or by optical radiation. In the examples described

3 herein, imaging of the photoresist was performed in a MEBES™ QUADRA™ electron

4 beam mask patterning system (available from ETEC Systems, Inc., an Applied Materials

5 company, with Applied Materials, Inc., having offices in Santa Clara, CA). Other imaging

6 systems which can be used to practice the method described herein include, without

7 limitation, the MEBES™ eXara™ electron beam mask patterning system, and the ALTA™

8 3900 and ALTA™ 4300 laser beam mask patterning systems (all available from ETEC

9 Systems, Inc.).

10 [0039]   After imaging of the photoresist on the photomask substrate, the imaged

11 photoresist was treated with a vacuum for a period of time sufficient to allow pattern critical

12 dimensions to reach equilibrium across a given photoresist layer. The time period required

13 for latent, imaged pattern critical dimensions to reach equilibrium across the photoresist will

14 depend upon a combination of the temperature of the substrate during the vacuum treatment

15 process and the pressure (vacuum) applied. After exposure of the imaged photoresist on the

16 photomask substrate to vacuum for an optimum time period, no substantial change in pattern

17 critical dimensions will occur upon continued exposure of the imaged photoresist to

18 vacuum.

19 [0040]   Typically, the higher the temperature, the less time is required for imaged pattern

20 critical dimensions to reach equilibrium. However, the temperature is limited by the general

21 stability of the photoresist material, which will depend on the particular photoresist material

22 used. Also, typically the lower the pressure in the process chamber, the less time is required

23 at a given temperature; however, the pressure used must ensure that deformation of the

24 pattern does not occur and that the integrity of the photoresist is preserved. The amount of

25 time required will also depend upon the condition of the photoresist prior to the vacuum

26 treatment process, which will depend upon the type of photoresist used, the solvents in the

27 photoresist, and the length of time of the post-apply bake (PAB) process. With minimal

28 experimentation, one skilled in the art will be able to determine the amount of time required

1   based on the particular apparatus that s/he is using and the particular process conditions

2   under which that apparatus typically operates.

3   [0041]   Vacuum treatment of photomask substrates in accordance with the methods of the

4   invention can be performed in any suitable semiconductor processing apparatus which is

5   capable of maintaining a process chamber pressure within the range of about 5×10^{-6} mTorr

6   to about 5 mTorr. For example, an imaged photomask substrate may be vacuum treated in

7   the exposure tool used for direct-write pattern irradiation of the photoresist. Alternatively,

8.   vacuum treatment of the imaged photomask substrates can be performed in other available

9   equipment, for example, and not by way of limitation, in an Applied Materials' TETRA™

10   photomask etch system. By moving the photomask substrates to a different chamber for

11   vacuum treatment following imaging, exposure tool throughput is not affected.

12   [0042]   Typically, exposure of the imaged photoresist on the photomask substrate to

13   vacuum is performed at a substrate temperature within the range of about 18°C to about

14   60°C (more typically, within the range of about 18°C to about 40°C. Heating of the imaged

15   resist on the photomask substrate to a temperature within the range of about 30°C to about

16   60°C, and at a pressure ranging from about 0.1 mTorr to about 5 mTorr provides a

17   substantial improvement in imaged resist pattern uniformity after a treatment .

18   [0043]   Figure 2 is a graph 200 showing global cross 1 x CD uniformity 202 (in nm)

19   following vacuum treatment of the imaged photoresist prior to development, where the

20   substrates were vacuum treated in the MEBES™ QUADRA™ imaging system ("RSB

21   Vacuum Treated") 204 or were vacuum treated in an Applied Materials' TETRA™ etch

22   chamber ("Tetra Vacuum Treated") 206, compared with the global CD uniformity for

23   substrates which received no vacuum treatment following exposure of the photoresist to

24   radiation ("No Vacuum") 208. The RSB Vacuum substrates were vacuum treated in the

25   pattern writing apparatus for a period of 5 - 9 hours at approximately 21 - 22°C), at a

26   process chamber pressure of approximately 1×10^{-5} mTorr. The Tetra Vacuum substrates

27   were vacuum treated in a TETRA™ etcher for a period of 30 minutes at a temperature of

28   approximately 30°C, at a process chamber pressure of approximately 1 mTorr The

1   substrates which received no vacuum treatment were maintained at approximately

2   21 - 22°C.

3   [0044]   After vacuum treatment, the photoresist was baked again. The second baking step

4   is typically referred to as a "post-exposure bake" or PEB. Chemical reaction takes place

5   between the time the pattern is written by irradiation upon the photoresist and the PEB, but

6   after the PEB, the latent image is essentially fixed within the photoresist. The amount of

7   time and the temperature of the substrate (*i.e.*, the time / temperature profile) depends on the

8   photoresist, and one skilled in the art can determine what this should be in view of the

9   photoresist manufacturer's recommendations.

10   [0045]   The post-exposure bake process is typically performed at a temperature within the

11   range of about 70°C to about 150°C, for a time period of about 4 minutes to about

12   30 minutes. A particularly useful post-exposure bake process is described in detail in U.S.

13   Patent No. 6,703,169, to Scott Fuller et al., the disclosure of which is incorporated by

14   reference in its entirety.

15   [0046]   After post-exposure bake, the photoresist is developed, either using a dry process

16   or a wet process, to create the pattern having openings through the photoresist layer

17   thickness. The photoresist in the present instance was developed using a puddle or spray

18   develop process with a TMAH (2.38 weight % or 1.91 weight %) developer.

19   [0047]   We have also discovered that exposure of the patterned (developed) photoresist

20   to vacuum after development results in an improvement in the line edge roughness of pattern

21   openings that have been formed through the photoresist layer thickness. Accordingly, after

22   development of the photoresist, the method of the invention may further comprise an

23   optional step of exposing the photoresist to a vacuum at a substrate temperature within the

24   range of about 20°C to about 60°C for a period of time within the range of about 10 minutes

25   · to about 60 minutes, at a process chamber pressure ranging from about 5×10^{-6} mTorr to

26   about 5 mTorr.

27   [0048]   In this second vacuum treatment, water vapor and solvents absorbed during the

28   development process are desorbed from surfaces of the patterned resist, including the

1   sidewalls and top resist surface. During desorption of the volatile components, the portion

2   of the resist which is close to the surface is placed in tension. It is theorized, but not

3   intended as a limitation, that this surface tension may allow for the "pulling together" of the

4   surface, which may smooth out sidewall roughness. Since the bulk of the resist (deeper than

5   within a few nanometers of the surface) is not in tension, lines and other features are not

6   distorted.

7   [0049]   Proper timing of the vacuum treatment process allows for desorption of water

8   vapor, solvents, and other by-products of previous processing steps from the surface of the

9   resist, and also enables acids within the resist to diffuse in such a way as to reduce line edge

10   roughness. Desorption of materials from the resist was found to slightly decrease the

11   thickness of the photoresist layer. In addition, a slight shrinkage of pattern dimension was

12   observed in the lateral (photomask plane) directions. Overall, vacuum processing of

13   photomask substrates according to the method of the invention typically improves the mean

14   CD of the patterned photoresist by reducing the variation of the intended CD by

15   approximately 3 nm or more, and by improving the uniformity (3 sigma) across the wafer

16   by about 3 - 5 nm. Our data also show an improvement in local CD uniformity.

17   [0050]   Figure 3 is a graph 300 showing the decrease in photoresist thickness 302 for a

18   developed photoresist as a function of time under vacuum 304 for photomask substrates

19   which were vacuum treated in accordance with the present invention. The "curve" 306 of

20   resist change is observed to "flatten out" (i.e., reach equilibrium) after about 20 minutes of

21   vacuum treatment, after which no substantial change in pattern critical dimensions was

22   observed upon continued exposure of the imaged photoresist to vacuum. The substrates

23   were vacuum treated in an Applied Materials' TETRA™ etch chamber for a period of 20

24   minutes, at a temperature of approximately 45°C, and a process chamber pressure of

25   approximately 0.5 mTorr.

26   [0051]   The data presented graphically in Figure 3 is for the REAP™ 200 photoresist.

27   Data were also obtained for the EN24 photoresist (available from TOK, Kawasaki, Japan)

28   and FEP 171 photoresist (available from Fuji-Hunt Electronics Company, Tokyo, Japan),

1   under the same processing conditions described above for the REAP™ 200 photoresist.

2   These data are presented in Table One, below.

3   [0052]   Table One. Decrease in Photoresist Thickness Following Post-Exposure
4   Vacuum Treatment

Photoresist	Decrease in Photoresist Thickness (Å)
REAP™ 200	20
EN24	23
FEP 171	17

9   [0053]   Figure 4 is a graph 400 showing local CD uniformity 402 (in nm) before ("PreVac

10   CDU") and after ("PostVac CDU") vacuum treatment of the developed photoresist. The

11   substrates were vacuum treated in an Applied Materials' TETRA™ etch chamber for 20

12   minutes, at a temperature of approximately 45°C and a process chamber pressure of

13   approximately 1 mTorr. Local CD variations for the y direction pre-vacuum treatment 404

14   and post-vacuum treatment 406 are shown for a first sample ("Sample # 1"). Local CD

15   variations for the y direction pre-vacuum treatment 408 and post-vacuum treatment 410, are

16   also shown for a second sample ("Sample # 2"). The two photomask substrate samples had

17   different line-and-space patterns, which would explain the variation in CD uniformity

18   between the two samples. The data shown in Figure 4 are for a REAP™ photoresist

19   (available from TOK, Kawasaki, Japan).

20   [0054]   In addition to their use in the preparation of photomasks, the vacuum treatment

21   processes described herein can be used to improve the quality of lithography in the

22   patterning of semiconductor wafers. The vacuum treatment processes described herein can

23   be applied to all wafer lithographic processes where critical dimension control is required,

24   for all wavelengths of light utilized in wafer optical and e-beam lithography (G-line, i-line,

25   KrF, ArF, 257 nm, for example, and not by way of limitation), plus other methods used for

26   patterning resist on wafers, such as EUV. Line edge roughness is reduced, and critical

1   dimension control is improved.

2   [0055]   Figure 1B shows a schematic cross-sectional view of the patterned photoresist

3   layer 108 (prior to transfer of the pattern through underlying organic ARC layer 106,

4   inorganic ARC layer 105, and chrome-containing layer 104), where the pattern was lines

5   107 and spaces 111, where the line width was about 30 nm to about 3 μm and the spacing

6   between lines was about 30 nm to about 3 μm.

7   [0056]   Once the photoresist has been developed and "patterned", so that the pattern

8   openings extend through the photoresist layer to the upper surface of an ARC layer, or to a

9   surface beneath an ARC layer, subsequent processing steps are typically performed in order

10   to transfer the pattern in the patterned photoresist through the chrome-based mask layer and

11   any remaining layers overlying the chrome layer. These subsequent processing steps are

12   summarized below and are also described in detail in U.S. Patent No. 6,703,169, to Scott

13   Fuller et al., which is incorporated by reference herein in its entirety. The mask fabrication

14   process transforms the latent image created by the exposure of the photoresist into a

15   permanent chrome image on the quartz substrate.

16   [0057]   The pattern in the photoresist is typically transferred to the underlying photomask

17   structure using a dry etch process, such as a plasma etching process. The chrome oxynitride

18   (inorganic ARC) / chrome mask layer etch is typically performed using a plasma generated

19   from a chlorine / oxygen / helium gas mixture. Typically, higher oxygen concentrations and

20   lower pressures cause higher mean-to-target deviation and lower selectivities, while favoring

21   better CD uniformity control. Plasma etch systems such as the TETRA™ etch system

22   (available from Applied Materials, Inc., of Santa Clara, CA) may be used to provide

23   excellent results. However, one skilled in the art will be able to optimize the process for

24   other plasma etch apparatus.

25   [0058]   Typically, the chrome layer is overetched beyond endpoint to clear residual

26   chrome from all open regions. Generally, the overetch step is an extension of the chrome

27   etch process described above. Longer overetch steps result in higher mean-to-target

28   deviations. Chrome spot defect densities can be affected by the length of overetch, with

1   lower defect densities for longer overetch processes.

2   [0059]   After completion of the chrome layer etch, a strip and clean process is typically

3   performed to remove any residual contaminants from the surface of the chrome layer. The

4   strip process may be performed by heating sulfur peroxide to about 75°C and applying the

5   heated sulfur peroxide over the surface of the substrate plate. After treatment with sulfuric

6   peroxide, the substrate plate is typically rinsed with CO_2-reionized or CO_2-sparged deionized

7   water. After strip, the substrate plate is typically subjected to an acid clean using an industry

8   standard 70 : 30 H_2SO_4 / H_2O_2 solution, followed by another deionized water rinse. For

9   example, the strip step may be performed on a Steag ASC 500 wet chemical processing

10   station, available from STEAG-HAMMATECH® (Santa Clara, CA).

11   [0060]   The above described preferred embodiments are not intended to limit the scope

12   of the present invention, as one skilled in the art can, in view of the present disclosure,

13   expand such embodiments to correspond with the subject matter of the invention claimed

14   below.